PATENT APPLICATION
DOCKET NO. BP3316

TITLE: METHOD FOR AVOIDING AVALANCHE BREAKDOWN CAUSED BY A LATERAL PARASITIC BIPOLAR TRANSISTOR IN AN MOS PROCESS

INVENTOR

Arya Reza Behzad

SPECIFICATION

Cross Reference to Related Application

This application claims priority to U.S. Provisional Patent Application Serial No. 60/510,826, filed October 14, 2003, which is incorporated herein by reference for all purposes.

BACKGROUND

1. Technical Field

This invention relates generally to communication systems and more particularly to power amplifiers used in transmitters within such communication systems.

2. Related Art

Communication systems are known to support wireless and wire lined communications between wireless and/or wire lined communication devices. Such communication systems range from national and/or international cellular telephone systems to the Internet to point-to-point in-home wireless networks. Communication systems typically operate in accordance with one or more communication standards. For instance, wired communication systems may operate according to one or more versions of the Ethernet standard, the System Packet Interface (SPI) standard, or various other standards. Wireless communication systems may operate in accordance with one or more standards including, but not limited to, IEEE 802.11, Bluetooth, advanced mobile phone

services (AMPS), digital AMPS, global system for mobile communications (GSM), code division multiple access (CDMA), local multi-point distribution systems (LMDS), multi-channel-multi-point distribution systems (MMDS), and/or variations thereof.

Depending on the type of wireless communication system, a wireless communication device, such as a cellular telephone, two-way radio, personal digital assistant (PDA), personal computer (PC), laptop computer, home entertainment equipment, et cetera communicates directly or indirectly with other wireless communication devices. Each wireless communication device participating in wireless communications includes a built-in radio transceiver (i.e., receiver and transmitter) or is coupled to an associated radio transceiver (e.g., a station for in-home and/or in-building wireless communication networks, RF modem, etc.). As is known, the transmitter includes a data modulation stage, one or more frequency conversion stages, and a power amplifier. The data modulation stage converts raw data into baseband signals in accordance with the particular wireless communication standard. The one or more frequency conversion stages mix the baseband signals with one or more local oscillations to produce RF signals. The power amplifier amplifies the RF signals prior to transmission via an antenna.

As compared/contrasted to the wireless communication device described above, a transmitter of a wired communication device includes a data modulation stage, the power amplifier and may include a frequency conversion stage that frequency converts a baseband signal produced by the data modulation stage to a transmit band. While power amplifiers of wired communication devices do not typically operate in the RF range, they have similar operational requirements. In both wired and wireless communication

devices, the power amplifier is often required to provide a high swing at its output. The power amplifier must also be very linear in its operation and also use as little power as possible. These competing goals are very difficult to meet, particularly in portable devices that are battery powered and that operate at relatively low voltages.

BRIEF SUMMARY OF THE INVENTION

A power amplifier constructed according to the present invention overcomes these and other shortcomings of the prior art devices and includes a transconductance stage, a cascode stage, and a connector. The transconductance stage is operable to receive an input voltage signal and to produce an output current signal. The cascode stage communicatively couples to the transconductance stage and is operable to receive the output current signal and to produce an output voltage signal based thereupon. The cascode stage includes a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar transistor formed in parallel therewith in a semi conductive substrate. The MOS transistor has a drain, a gate, and a source. The corresponding parasitic bipolar junction transistor has a collector corresponding to the drain, an emitter corresponding to the source, and a base corresponding to the semi conductive substrate. The connector couples the base of the corresponding parasitic bipolar junction transistor to the source of the MOS transistor.

In one embodiment, the MOS transistor includes an N type source and an N type drain formed in a P type substrate to define a channel there between and a gate formed upon the P type substrate above the channel. The corresponding parasitic bipolar junction transistor has an emitter corresponding to the N type source, a collector

corresponding to the N type drain, and a base corresponding to the P type substrate. This embodiment further includes a P+ base contact corresponding to the parasitic bipolar transistor formed in the P type substrate. The connector couples the P+ base contact to the N type source .

In another embodiment, the MOS transistor includes a P type source and a P type drain formed in an N type substrate to define a channel there between and a gate formed upon the N type substrate above the channel. The corresponding parasitic bipolar junction transistor includes an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate. This embodiment further includes an N+ base contact corresponding to the parasitic bipolar transistor formed in the N type substrate. The connector couples the N+ base contact to the P type source.

In one embodiment, the semi conductive substrate is a well formed in a semi conductive wafer and the connector couples between the well and the source, which is formed in the well. With this structure, a base contact is formed in the well. The connector may be formed in a low metal layer to minimize its resistance. The power amplifier may further include a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor.

In one construct, the transconductance stage includes a transconductance element having a first terminal tied to ground and a second terminal. With this construct, the MOS transistor and the corresponding bipolar junction transistor of the cascode stage include a shared first terminal and a shared second terminal coupled to the second

terminal of the transconductance element. This construct further includes a circuit element coupled between a voltage source and the shared first terminal of the MOS transistor and the corresponding bipolar junction transistor.

In another construct, the transconductance stage includes a transconductance element and a circuit element that couple in series between a transconductance stage voltage source and ground. With this construct, the cascode stage includes a first circuit element having a first terminal coupled to ground and a second terminal and a second circuit element having a first terminal tied to a cascode stage voltage supply and a second terminal. The MOS transistor and the corresponding bipolar junction transistor couple between the second terminal of the first circuit element and the second terminal of the second circuit element. This construct further includes an AC coupling stage that couples the output current signal produced by the transconductance stage to the cascode stage. With either of these constructs, the transconductance element may be selected from the group consisting of transistors and linearized transconductance stages.

Other features and advantages of the present invention will become apparent from the following detailed description of the invention made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram illustrating a wireless communication system in accordance with the present invention;

FIG. 2 is a schematic block diagram illustrating a wireless communication device in accordance with the present invention;

FIG. 3 is a schematic diagram illustrating a singled ended cascode power amplifier;

FIG. 4 is a schematic diagram illustrating a single ended cascode power amplifier constructed according to the present invention;

FIG. 5 is a schematic diagram illustrating a differential cascode power amplifier constructed according to the present invention;

FIG. 6 is a schematic diagram illustrating a differential cascode power amplifier having variable cascode stage biasing according to the present invention.

FIG. 7 is a schematic diagram illustrating a differential cascode power amplifier with a structure similar to that of FIG. 6 but that employs a linearized transconductance stage;

FIG. 8 is a block diagram illustrating a linearized transconductance stage that may be employed with a power amplifier constructed according to an embodiment of the present invention;

FIG. 9 is a schematic block diagram illustrating a first particular embodiment of the linearized transconductance stage of FIG. 8;

FIG. 10A is a schematic block diagram illustrating a second particular embodiment of the linearized transconductance stage of FIG. 8;

FIG. 10B is a schematic diagram illustrating another embodiment of the biasing circuit of FIG. 8;

FIG. 11 is a schematic diagram illustrating a power amplifier having modulation dependent transconductance stage biasing;

FIG. 12 is a graph illustrating one technique for adjusting a power amplifier bias voltage according to an embodiment of the present invention;

FIG. 13 is a flow chart illustrating operation according to one embodiment of the present invention in adjusting a bias level of a power amplifier;

FIG. 14 is a cross-section taken along the channel of an N-type Metal-Oxide-Silicon (NMOS) transistor illustrating a parasitic NPN bipolar transistor formed therewith according to the present invention;

FIG. 15 is a schematic diagram illustrating a technique for tying a base of a parasitic NPN bipolar transistor to ground via an external resistance;

FIG. 16 is a cross-section taken along the channel of an N-type Metal-Oxide-Silicon (NMOS) transistor illustrating a parasitic NPN bipolar transistor having its base directly coupled to a source of the NMOS transistor according to the present invention;

FIG. 17 is a schematic diagram illustrating a first embodiment of a singled ended cascode power amplifier having a parasitic NPN bipolar transistor terminated according to the present invention; and

FIG. 18 is a schematic diagram illustrating a second embodiment of a singled ended cascode power amplifier having a parasitic NPN bipolar transistor terminated according to the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram illustrating a communication system 10 that includes a plurality of base stations and/or access points 12-16, a plurality of wireless communication devices 18-32 and a network hardware component 34. The wireless

communication devices 18-32 may be laptop host computers 18 and 26, personal digital assistant hosts 20 and 30, personal computer hosts 24 and 32, cellular telephone hosts 22 and 28, and/or any other type of device that supports wireless communications. The details of the wireless communication devices will be described with reference to FIG. 2.

The base stations or access points 12-16 are operably coupled to the network hardware 34 via local area network connections 36, 38 and 40. The network hardware 34, which may be a router, switch, bridge, modem, system controller, et cetera provides a wide area network connection 42 for the communication system 10. Each of the base stations or access points 12-16 has an associated antenna or antenna array to communicate with the wireless communication devices in its area. Typically, the wireless communication devices register with a particular base station or access point 12-14 to receive services from the communication system 10. For direct connections (i.e., point-to-point communications), wireless communication devices communicate directly via an allocated channel.

Typically, base stations are used for cellular telephone systems and like-type systems, while access points are used for in-home or in-building wireless networks. Regardless of the particular type of communication system, each wireless communication device includes a built-in radio and/or is coupled to a radio. The radio includes a highly linear amplifiers and/or programmable multi-stage amplifiers as disclosed herein to enhance performance, reduce costs, reduce size, and/or enhance broadband applications.

FIG. 2 is a schematic block diagram illustrating a wireless communication device that includes the host device 18-32 and an associated radio 60. For cellular telephone hosts, the radio 60 is a built-in component. For personal digital assistants hosts, laptop

hosts, and/or personal computer hosts, the radio 60 may be built-in or may be an externally coupled component that couples to the host device 18-32 via a communication link, e.g., PCI interface, PCMCIA interface, USB interface, or another type of interface.

As illustrated, the host device 18-32 includes a processing module 50, memory 52, radio interface 54, input interface 58 and output interface 56. The processing module 50 and memory 52 execute the corresponding instructions that are typically done by the host device. For example, for a cellular telephone host device, the processing module 50 performs the corresponding communication functions in accordance with a particular cellular telephone standard.

The radio interface 54 allows data to be received from and sent to the radio 60. For data received from the radio 60 (e.g., inbound data), the radio interface 54 provides the data to the processing module 50 for further processing and/or routing to the output interface 56. The output interface 56 provides connectivity to an output display device such as a display, monitor, speakers, et cetera such that the received data may be displayed. The radio interface 54 also provides data from the processing module 50 to the radio 60. The processing module 50 may receive the outbound data from an input device such as a keyboard, keypad, microphone, et cetera via the input interface 58 or generate the data itself. For data received via the input interface 58, the processing module 50 may perform a corresponding host function on the data and/or route it to the radio 60 via the radio interface 54.

Radio 60 includes a host interface 62, digital receiver processing module 64, an analog-to-digital converter 66, a filtering/gain/attenuation module 68, an IF mixing down conversion stage 70, a receiver filter 71, a low noise amplifier 72, a transmitter/receiver

switch 73, a local oscillation module 74, memory 75, a digital transmitter processing module 76, a digital-to-analog converter 78, a filtering/gain/attenuation module 80, an IF mixing up conversion stage 82, a power amplifier 84, a transmitter filter module 85, and an antenna 86. The antenna 86 may be a single antenna that is shared by the transmit and receive paths as regulated by the Tx/Rx switch 77, or may include separate antennas for the transmit path and receive path. The antenna implementation will depend on the particular standard to which the wireless communication device is compliant.

The digital receiver processing module 64 and the digital transmitter processing module 76, in combination with operational instructions stored in memory 75, execute digital receiver functions and digital transmitter functions, respectively. The digital receiver functions include, but are not limited to, digital intermediate frequency to baseband conversion, demodulation, constellation demapping, decoding, and/or descrambling. The digital transmitter functions include, but are not limited to, scrambling, encoding, constellation mapping, modulation, and/or digital baseband to IF conversion. The digital receiver and transmitter processing modules 64 and 76 may be implemented using a shared processing device, individual processing devices, or a plurality of processing devices. Such a processing device may be a microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions. The memory 75 may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static

memory, dynamic memory, flash memory, and/or any device that stores digital information. Note that when the processing module 64 and/or 76 implements one or more of its functions via a state machine, analog circuitry, digital circuitry, and/or logic circuitry, the memory storing the corresponding operational instructions is embedded with the circuitry comprising the state machine, analog circuitry, digital circuitry, and/or logic circuitry. The memory 75 stores, and the processing module 64 and/or 76 executes, operational instructions that facilitate functionality of the device. In some embodiments, the combination of the digital receiver processing module, the digital transmitter processing module, and the memory 75 may be referred to together as a "baseband processor."

In operation, the radio 60 receives outbound data 94 from the host device via the host interface 62. The host interface 62 routes the outbound data 94 to the digital transmitter processing module 76, which processes the outbound data 94 in accordance with a particular wireless communication standard (e.g., IEEE802.11a, IEEE802.11b, IEEE802.11g, Bluetooth, et cetera) to produce digital transmission formatted data 96. The digital transmission formatted data 96 will be a digital base-band signal or a digital low IF signal, where the low IF typically will be in the frequency range of one hundred kilohertz to a few megahertz.

The digital-to-analog converter 78 converts the digital transmission formatted data 96 from the digital domain to the analog domain. The filtering/gain/attenuation module 80 filters and/or adjusts the gain of the analog signal prior to providing it to the IF mixing stage 82. The IF mixing stage 82 directly converts the analog baseband or low IF signal into an RF signal based on a transmitter local oscillation 83 provided by local

oscillation module 74. The power amplifier 84 amplifies the RF signal to produce outbound RF signal 98, which is filtered by the transmitter filter module 85. The antenna 86 transmits the outbound RF signal 98 to a targeted device such as a base station, an access point and/or another wireless communication device.

The radio 60 also receives an inbound RF signal 88 via the antenna 86, which was transmitted by a base station, an access point, or another wireless communication device. The antenna 86 provides the inbound RF signal 88 to the receiver filter module 71 via the Tx/Rx switch 77, where the Rx filter 71 bandpass filters the inbound RF signal 88. The Rx filter 71 provides the filtered RF signal to low noise amplifier 72, which amplifies the signal 88 to produce an amplified inbound RF signal. The low noise amplifier 72 provides the amplified inbound RF signal to the IF mixing module 70, which directly converts the amplified inbound RF signal into an inbound low IF signal or baseband signal based on a receiver local oscillation 81 provided by local oscillation module 74. The down conversion module 70 provides the inbound low IF signal or baseband signal to the filtering/gain/attenuation module 68. The filtering/gain/attenuation module 68 may be implemented in accordance with the teachings of the present invention to filter and/or attenuate the inbound low IF signal or the inbound baseband signal to produce a filtered inbound signal.

The analog-to-digital converter 66 converts the filtered inbound signal from the analog domain to the digital domain to produce digital reception formatted data 90. The digital receiver processing module 64 decodes, descrambles, demaps, and/or demodulates the digital reception formatted data 90 to recapture inbound data 92 in accordance with the particular wireless communication standard being implemented by radio 60. The host

interface 62 provides the recaptured inbound data 92 to the host device 18-32 via the radio interface 54.

As one of average skill in the art will appreciate, the wireless communication device of FIG. 2 may be implemented using one or more integrated circuits. For example, the host device may be implemented on one integrated circuit, the digital receiver processing module 64, the digital transmitter processing module 76 and memory 75 may be implemented on a second integrated circuit, and the remaining components of the radio 60, less the antenna 86, may be implemented on a third integrated circuit. As an alternate example, the radio 60 may be implemented on a single integrated circuit. As yet another example, the processing module 50 of the host device and the digital receiver and transmitter processing modules 64 and 76 may be a common processing device implemented on a single integrated circuit. Further, the memory 52 and memory 75 may be implemented on a single integrated circuit and/or on the same integrated circuit as the common processing modules of processing module 50 and the digital receiver and transmitter processing module 64 and 76.

FIG. 3 is a schematic diagram illustrating a singled ended cascode power amplifier 300. The single ended cascode power amplifier 300 includes a transconductance stage having a transistor M1 that receives an input voltage signal and produces an current signal through the transistor M1. Transistor M1 is biased in its active range by inductor L0 and the voltage drop across cascode transistor M0. The cascode transistor M0 is biased by the V_{bc} voltage level to control the impedance at node 302. An output voltage at node 302 is a product of the current that passes through transistors M1 and M0 and the impedance at node 302.

Cascode amplifiers provide various advantages when used as power amplifiers in a transmitter, e.g., RF Power Amplifier 84 of FIG. 2, a power amplifier of a wired communication device, etc. One advantage to using a cascode amplifier as a power amplifier is so that a relatively high voltage supply avdd1 may be employed in combination with a fine-geometry, low-voltage, high-Gm device, i.e., transistor M1. In the configuration of FIG. 3, the cascode device M0 tolerates the high voltage swing at the node 302, and the low-voltage M1 transistor provides the transconductance or gain. In this way, the large Gm for a given bias current can be achieved and a large swing can be tolerated without damage to the low voltage device M1 transistor. The cascode transistor M0 also assist in reducing the Miller effect experienced by the transconductance transistor M1.

The cascode configuration provides additional benefits as well. The cascode power amplifier 300 provides excellent input/output isolation to reduce or eliminate oscillations between the input side of the amplifier and the output side of the amplifier. Such isolation assists in facilitating proper tuning of the amplifier as well as circuits on the input side and the output side of the amplifier.

The cascode power amplifier 300 of FIG. 3, however does not allow for maximum possible headroom. "V_{bc}" has to be tied to a bias line in such a way that transistor M1 has sufficient V_{ds} drop so that it may provide reasonably high Gm and reasonably high output impedance (R_o). Further, V_{bc} must be low enough so that the cascode device M0 has enough V_{ds} drop so that it does not suffer from low and signal dependent output impedance and a resulting loss of gain and linearity.

FIG. 4 is a schematic diagram illustrating a single ended cascode power amplifier 400 constructed according to the present invention. The power amplifier includes a transconductance stage 402, a cascode stage 404, and an AC coupling element 406. The transconductance stage 402 receives an input voltage signal (V_{in}) and produces an output current signal. The transconductance stage 402 comprises a series combination of a linear transconductance element M3 and a circuit element L1 coupled between a transconductance stage voltage supply avdd1 and a ground. In the embodiment of FIG. 4, the linear transconductance element M3 comprises a transistor and the circuit element comprises an inductor L1. A first terminal of the inductor L1 couples to the transconductance stage voltage supply avdd1, a second terminal of the inductor couples to a drain of the transistor M3, a source of the transistor couples to a ground, and the input voltage signal Vin couples to a gate of the transistor M3. Thus, the inductor L1 is in series with the source and drain terminals of the transistor M3. The transistor M3 may be one of a metal oxide silicon field effect (MOSFET) transistor, a field effect transistor, and a bipolar junction transistor, and is a MOSFET in the illustrated embodiment.

The AC coupling element 406 couples between the transconductance stage 402 and the cascode stage 404 and AC couples the output current signal of the transconductance stage 402 produced at node 408 as the input current signal of the cascode stage 404 at node 410. In the illustrated embodiment, the AC coupling element 406 is a capacitor.

The cascode stage 404 is adapted to receive an input current signal at node 410 and to produce an output voltage signal Vout. In the illustrated embodiment, the cascode stage includes a series combination of a first circuit element (inductor L3) , source and

drain terminals of a transistor M4, and a second circuit element (inductor L2), the series combination biased between a cascode stage voltage supply avdd2 and a ground. A gate of the transistor M4 is adapted to receive a controllable cascode bias voltage V_{bc}. As will be described further with reference to FIGs. 6 and 7, in some embodiments, V_{bc} is varied depending upon the operating conditions of the transmitter serviced by the power amplifier 400. In other embodiments, V_{bc} is fixed.

In operation, Vout has an operational range extending from less than ground to greater than the cascode supply voltage avdd2. The transconductance stage 402 and the cascode stage 404 may be powered at differing voltage supply levels, e.g., avdd2<>avdd1, or may be powered at a common voltage supply level, e.g., avdd2=avdd1.

With the cascode amplifier 400 of FIG. 4, the transconductance stage 402 is effectively decoupled from the cascode stage 404 by the AC coupling element 406 (capacitor C0) and inductors L1 and L2. Inductors L1 and L2 may be large enough to act as a choke or, alternately, may be chosen to resonate out load capacitances at their respective nodes. Either way the signal current flows through the C0 cap and through M4 and to the load inductor L3. With this scheme, not only can the output voltage Vout swing above cascode supply voltage avdd2, but also the source of the M4 cascode device can swing below ground (gnd) providing a very large possible swing across the M4 device. Since M3 is a low voltage device, it can be fed from the lower voltage supply avdd1 (e.g. 1.8V) while the cascode stage 404 can be fed from a higher voltage supply avdd2 (e.g. 3.3V) for maximum possible swing.

For power amplifiers, maximum swing is desirable. Lower swing can typically be tolerated if high-ratio impedance transformers are used but such transformers are typically either not available at frequencies or lossy. The power consumption of the circuit of FIG. 4 is more than that of FIG. 3 for the same gain level. However, the circuit of FIG. 4 produces output power levels that cannot be achieved by the circuit of FIG. 3.

FIG. 5 is a schematic diagram illustrating a differential cascode power amplifier 500 constructed according to the present invention. The differential power amplifier 500 includes a differential transconductance stage (504a and 504b), a differential cascode stage (502a and 502b), and a differential AC coupling element (506a and 506b). The differential transconductance stage (504a and 504b) is adapted to receive a differential input voltage signal (Vin1 and Vin2) and to produce a differential output current signal. The differential cascode stage (502a and 502b) is adapted to receive a differential input current signal and to produce a differential output voltage signal (Vout1 and Vout2). The differential AC coupling element (506a and 506b) couples between the differential transconductance stage (502a and 502b) and the differential cascode stage (504a and 504b) and operates to AC couple the differential output current signal of the differential transconductance stage (402a and 402b) as the differential input current signal of the differential cascode stage. In the illustrated embodiment, each AC coupling element 506a and 506b of the differential AC coupling element is a capacitor. In operation, the differential output voltage signal is amplified with respect to the differential input voltage signal.

Each portion of the differential transconductance stage 502a (502b) includes a series combination of a linear transconductance element M3 (M6) and a circuit element

L1 (L6) coupled between a transconductance stage voltage supply avdd1 and a ground. In the illustrated embodiment, each linear transconductance element comprises a transistor M3 (M6) and each circuit element comprises an inductor L1 (L6). As illustrated, for each series combination, the inductor is in series with source and drain terminals of the corresponding transistor.

Each portion of the differential cascode stage 504a (504b) comprises a series combination of a first inductor L3 (L4), a transistor M4 (M5), and a second inductor L2 (L5) biased between a cascode stage voltage supply avdd2 and a ground. In this structure, for each portion of the differential cascode stage 504a (504b), gates of each transistor M4 (M5) are adapted to receive a controllable cascode bias voltage. Further, the differential transconductance stage 502a and 502b and the differential cascode stage 504 and 504b may be powered at differing voltage levels. Alternately, the differential transconductance stage 502a and 502b and the differential cascode stage 504 and 504b may be powered at a common voltage level. As illustrated inductors L2 (L5) and L3 (L4) are in series with source and drain terminals of transistor M4 (M5) such that the series combination of these elements couples between the cascode stage voltage supply avdd2 and ground.

FIG. 6 is a schematic diagram illustrating a differential cascode power amplifier 600 having variable cascode stage biasing constructed according to the present invention. The differential cascode power amplifier 600 includes a left portion 602a and a right portion 602b, a peak detector and low pass filter circuit 604, and a Vbias determination module 606. The left portion 602a and right portion 602b are similar to or the same as

corresponding components that are illustrated and discussed with reference to FIG. 5 but that have been modified according to the additional structure of FIG. 6.

The peak detector and low pass filter circuit 604 measures the signal level of an output voltage signal Vout1 and Vout2 produced by a differential transconductance stage of the differential power amplifier. Alternately, the peak detector and low pass filter circuit 604 measures the signal level of the input voltage signal Vin1 and Vin2. Based upon the level of the monitored signal, the peak detector and low pass filter circuit 604 produces a signal level output. The signal level output is representative of a modulated signal that is being operated upon by the power amplifier. The Vbias determination module 606 receives the signal level output and, based upon the signal level output, produces a V_{bc} voltage that is employed to bias each side of the differential cascode stage of the differential cascode power amplifier 600. Together, the peak detector and low pass filter 604 and the V_{bc} determination module 606 may be referred to as a modulation detection and bias determination module. The modulation detection and bias determination module may also be employed to produce a V_{bc} voltage for a single ended cascode power amplifier, such as is shown in FIG. 4 where V_{bc} is not fixed, which will be described further with reference to FIGs. 11 and 12.

Linear and amplitude dependent modulation schemes require very linear amplification of the incoming signal while also servicing a very large peak to average ratio. Meeting these requirements has previously required that the power amplifier be biased in the power hungry class A or AB region that only occasionally consumes a large bias current when the peaks of the modulation occur. The occurrence of these peaks is infrequent and is dependent on the statistics of the particular modulation used. However

ignoring these peaks would result in a poor amplification quality and a resultant poor error-vector magnitude.

The scheme of FIG. 6 utilizes the peak detector and low pass filter circuit 604 to estimate the input signal level, which is representative of the modulation. The signal level is then filtered and applied to the Vbias determination module 606 as the signal level output for adjusting the fixed level of V_{bc} as well as the signal dependent part of V_{bc}. The resultant V_{bc} signal is then applied to the gates of the cascode transistors M4 and M5. This scheme can produce a dramatic reduction in power consumption of the amplifier when used with high-linearity high peak-to-average ratio modulation schemes. Such structure and operation can increase the P1 dB of the operation of the power amplifier 600 in some cases.

In other embodiments, an envelope detector or another circuit that corresponds to an employed modulation scheme may replace the peak detector and low pass filter 604. When the serviced device supports differing modulation schemes, the operation of the peak detector and low pass filter 604 and the Vbias determination module 606 may be tailored to the modulation scheme employed in order to properly bias the cascode stage.

FIG. 7 is a schematic diagram illustrating a differential cascode power amplifier with a structure similar to that of FIG. 6 but that employs a linearized transconductance stage. As compared to the structure of FIG. 6, linearized transconductance stages 704a and 704b replace the transistor M3/M6 and inductor L1/L6 combinations. The peak detector and LPF 604 monitors either the Vin1/Vin2 signal pair and/or the outputs of the linearized transconductance stages 704a/704b. Particular examples of these linearized

transconductance stages 704a/705b will be described further with reference to FIGs. 8-10B.

FIG. 8 is a block diagram illustrating a linearized transconductance stage that may be employed with a power amplifier constructed according to an embodiment of the present invention. As shown in FIG. 8, a linearized transconductance stage 800 includes a primary transconductance stage 802, secondary transconductance stage 804, and a biasing circuit 814. The biasing circuit 814 generates a primary bias voltage 803 and a secondary bias voltage 805. The primary bias voltage 803 may be greater than the secondary bias voltage 805 such that the primary transconductance stage 802 becomes active before the secondary transconductance stage 804 becomes active. The particular operations of the linearized transconductance stage 800 are described in further detail in patent No. 6,496,067, issued 12/17/2002, which has common inventorship and a common assignee.

In operation, the primary transconductance stage 802 and the secondary transconductance stage 804 operably couple to receive the input voltage 806. Based on the primary bias voltage 803, the primary transconductance stage 802 converts the input voltage 806 into a primary current 808. The secondary transconductance stage 804 converts the input voltage 806 into a secondary current 810 based on the secondary bias voltage 805. The sum of the primary current 808 and the secondary current 810 produce an output current 812.

The biasing circuit 814, which may receive an input from the modulation detection and bias determination module, can dynamically add (or subtract) the output of the secondary transconductance stage 804 from the output of the primary

transconductance stage 802 to obtain a wider and more linear transconductance range. As such, the transconductance gain of each stage 802 and 804 are added based on the bias voltages produced by the biasing circuit 814. As the input voltage 806 increases in magnitude, the secondary transconductance stage 804 is turned on and broadens the effective transconductance linear range of the linearized transconductance stage 800. As one of average skill in the art will appreciate, the current produced by the secondary transconductance stage 804 may effectively be subtracted from the current produced by the primary transconductance stage 802 to compensate for ripple variations in the overall transconductance transfer function of the transconductance stage 800. A linearization offset voltage of the transconductance stage can be selected large enough to cause a gain expansion (pre-distortion) in the generated output current as a result of the applied input voltage. This gain expansion can then be used to partially compensate for the gain compression that would be inherent in the output (cascode) stage because of headroom limitations. This can increase the 1-dB compression point of the overall amplifier and its linear operating range. The concepts illustrated in FIG. 8 apply equally well to a differential implementation.

FIG. 9 is a schematic block diagram illustrating a first particular embodiment of the linearized transconductance stage 800 of FIG. 8. The linearized transconductance stage 900 includes a primary transconductance stage 802, a secondary transconductance stage 804, and a biasing circuit 814. The biasing circuit 814 may be part of, or operate complementary to the signal level detection and bias determination module illustrated previously with reference to FIGs. 6 and 7. The biasing circuit 814 includes current source 902 and transistor 904 and produces a reference voltage source (V_{ref}). The biasing

circuit 814 also includes a resistive pair (resistors 906 and 908) and voltage offset modules 910 and 912. In this configuration, the biasing circuit 814 provides the reference voltage (V_{ref}) as the primary bias voltage 914 to the primary transconductance stage 802.

The voltage offset modules 910 and 912 subtract an offset voltage (V_{os}) from the reference voltage (V_{ref}). The resulting voltage (V_{ref} - V_{os}) is provided as the secondary bias voltage 916 to the secondary transconductance stage 804. Such an offset may be created by a diode, a battery, a biased transistor, etc.

The primary transconductance stage 802 includes a 1st transistor 918 and a 2nd transistor 920. The 1st transistor 918 is operably coupled via capacitor 922 to receive one leg (e.g., V_{in}-) of a differential input voltage 926 (differential version of input voltage 806 of FIG. 8). The 2nd transistor 920 is operably coupled via capacitor 924 to receive a 2nd leg (e.g., V_{in}+) of the differential input voltage 926. As configured, the primary transconductance stage 802 produces a primary differential current 808 from the differential input voltage 926 based on the primary bias voltage 914. Accordingly, the primary bias voltage 914 is set to a level that insures that for almost any differential input voltage 926 a primary differential current 808 is produced.

The secondary transconductance stage 804 includes a 1st transistor 922 and a 2nd transistor 924. The gate voltage of transistors 922 and 924 is based on the secondary bias voltage 916 and the differential input voltage 926. For instance, the gate voltage for one transistor is $V_{ref} - V_{os}$ + delta V_{in}, while the gate voltage for the other transistor is $V_{ref} - V_{os}$ - delta V_{in}. When the gate threshold voltage of one of the transistors 922 and 924 is

exceeded, the secondary transconductance stage 804 generates the secondary differential current 810.

The output current 812 is the sum of the secondary differential current 810 and the primary differential current 808. Note that when the gate voltage on transistors 922 and 924 have not exceeded their threshold voltage, no secondary differential current 810 is produced. Thus, for relatively low differential input voltages 926, the output current 812 is produced solely by the primary differential current 808. As the magnitude of the differential input voltage 926 increases, the secondary transconductance stage 804 becomes active and generates the secondary differential current 810 which is added to the primary differential current 808 to produce the resulting output current 812, which improves the overall transconductance and linearity of the linearized transconductance stage 900.

FIG. 10A is a schematic block diagram illustrating a second particular embodiment of the linearized transconductance stage 800 of FIG. 8. The linearized transconductance stage 1000 of FIG. 10A includes an alternate embodiment of the primary transconductance stage 802, an alternate embodiment of the secondary transconductance stage 804, and the biasing circuit 814 (not shown). The biasing circuit 814, as previously discussed with reference to FIG. 9, produces a secondary bias voltage 916 and a primary bias voltage 914. The differential input voltage 926 is operably coupled to the primary transconductance stage 802 via capacitors 1002 and 1004 and to the secondary transconductance stage 804 via capacitors 1006 and 1008.

The primary transconductance stage 802 includes a 1st cascoded transistor pair 1010 and 1012 and a 2nd cascoded transistor pair 1014 and 1016. Transistors 1012 and

1016 are operably coupled to receive a bias voltage (V_{bx}). The inclusion of the cascoded transistors 1012 and 1016 improves performance in at least some applications. The cascoded transistors 1012 and 1016 provide isolation from the secondary transconductance stage 804. The bias voltage V_{bx} may be applied by the signal level detection and bias determination module that was previously described with reference to FIGs. 6 and 7 or may be applied by another circuit, e.g., a circuit illustrated in FIG. 10B.

The secondary transconductance stage 804 includes a 1st cascoded transistor pair 1018 and 1020 and a 2nd cascoded transistor pair 1022 and 1024. The cascoded transistors 1020 and 1024 are operably coupled to the transistor bias voltage (V_{bx}).The cascoded transistors 1020 and 1024 provide isolation from the primary transconductance stage 802.

As configured, the primary transconductance stage 802 produces the primary differential current 808 and the secondary transconductance stage 804 produces the secondary differential current 810. The output current 812 is the sum of the primary differential current 808 and the secondary differential current 810. As previously discussed, the secondary transconductance stage 804 does not immediately produce the secondary differential current 810. The secondary differential current 810 is produced when the differential input voltage 926 in combination with the secondary bias voltage 916 exceeds the threshold voltage of transistors 1018 and 1022.

FIG. 10B is a schematic diagram illustrating another embodiment of the biasing circuit 814 of FIG. 8. The biasing circuit 814 of FIG. 10B may be employed instead of the biasing circuit of FIG. 9 in biasing the linearized transconductance stage 1000 of FIG. 10A. The biasing circuit includes current sources 1052 and 1054, resistor 1056, and

transistor 1058. The transistor 1058 has its drain and source terminals tied at produces the primary bias voltage 914. The secondary bias voltage 916 is produced at the junction of resistor 1056 and current source 1054.

FIG. 11 is a schematic diagram illustrating a power amplifier 1100 having modulation dependent transconductance stage biasing. The power amplifier 1100 includes a power amplifier driver 1102, capacitor 1104, transconductance device 1108, cascode transistor 1110, and inductor 1112. The power amplifier 1100 also includes a peak detector and LPF 604, vbias determination module 606, and resistor 1106 that produce the transconductance stage bias voltage (V_{bt}). In an illustrated embodiment of the power amplifier 1100, V_{bc} is fixed (as it may be biased by the biasing circuit 814 of FIG. 10B). One variation of the power amplifier 1100 of FIG. 11 includes varying both V_{bt} and V_{bc} based upon the level of V_{in} to alter the operational characteristics of the power amplifier 1100. Another variation includes replacing the resistor 1106 with an inductor or another circuit element.

The manner in which the transconductance stage bias voltage V_{bt} is varied based upon the level of the input signal V_{in} is similar to the manner in which the cascode stage bias voltage V_{bt} is varied based upon the level of the input signal as was described with reference to FIG. 7. One particular technique for varying V_{bt} and/or V_{bc} will be described further with reference to FIG. 12.

With one variations of the power amplifier 1100, an inductor replaces the resistor 1106. With another variation of the power amplifier 1100, cascode transistor 1110 is eliminated. In another variation of the power amplifier 1100, transistor 1108 is degenerated using a resistor and/or an inductor. Further, the transistor 1108 may be

replaced by a linearized transconductance stage as described with reference to FIGs. 8-10B. A differential version of the power amplifier 1100 may be constructed in a straightforward manner, similar to the constructs previously described.

FIG. 12 is a graph illustrating one technique for adjusting a power amplifier bias voltage according to an embodiment of the present invention. As is shown, the bias voltage (V_{bc}, V_{bx}, V_{bt}, V_{REF} and/or V_B) applied to a transconductance stage and/or to a cascode stage is dependent upon a detected/measured signal level, e.g., Power in (Pin), Voltage in (Vin), Current in (Iin), etc. that is representative of a serviced modulation characteristic. Generally, the bias voltage does not go below a minimum level Vbias(min) or extend above a maximum level Vbias(max). When operating between Vbias(min) and Vbias(max), the bias voltage may vary linearly or non-linearly with the measured signal level. The slope or characterization of this curve may be fixed or may be variable depending upon the particular implementation. The selection of the minimum level, the maximum level, and the slope there between may be selected based upon the modulation type(s) serviced by the power amplifier, e.g., BPSK, GMSK, QPSK, 8PSK, 16QAM, 32QAM 64QAM, 128QAM, 256QAM, 512QAM, 1024QAM, etc.

Illustrated particularly in FIG. 12 are three relationships between input signal level and power amplifier bias voltage. A first relationship is linear and has a Slope B. The second relationship (C) is non linear. The third relationship (D) is also non-linear. Note that each of these relationships, be they linear or non-linear, extend from Vbias(min) to Vbias(max) over a range of input signal level. The reader should note that the input signal level at which the power amplifier bias voltage extends from Vbias(min)

and the input signal level at which the power amplifier bias voltage meets Vbias(max) is programmable/configurable at the Vbias determination module.

FIG. 13 is a flow chart illustrating operation according to one embodiment of the present invention in adjusting a bias level of a power amplifier. At step 1302 the modulation characteristics of a signal operated upon by the power amplifier are monitored. When such monitoring indicates that the modulation power (power of modulation envelope) increases by a threshold/exceeds a threshold (step 1304), the bias of the power amplifier is increased (step 1306). When such monitoring indicates that the modulation power (power of modulation envelope) decreases by a threshold/moves below a threshold (step 1308), the bias of the power amplifier is decreased (step 1310). Such an increase/decrease in the bias of the power amplifier may be caused using one of the techniques previously described with reference to FIGs. 5-12 or by another technique. From steps 1306 and 1310, operation returns to step 1302.

FIG. 14 is a cross-section taken along the channel of an N-type Metal-Oxide-Silicon (NMOS) transistor illustrating a parasitic NPN bipolar transistor 1414 formed therewith according to the present invention. The NMOS transistor 1404 is formed in a p-well 1402, which is formed either in an N-substrate 1400 or in an N-well in a P-type substrate (not shown). The NMOS transistor 1404 has a conventional structure with an N+ source 1406, an N+ drain 1410, a channel defined there between in the P-well 1402, and a gate 1408 having a gate conductor and an insulative gate oxide formed between the channel and the gate conductor. The parasitic NPN bipolar transistor 1414 is a byproduct of the structure of the NMOS transistor 1404. The parasitic NPN bipolar transistor 1414 has an emitter that corresponds to the source 1406 of the NMOS transistor 1404 and a

collector that corresponds to the drain 1410 of the NMOS transistor 1404. A base of the NPN bipolar transistor 1414 corresponds to the p-well 1402 in which the NMOS transistor 1404 is formed. Thus, the collector and emitter terminals of the parasitic NPN bipolar transistor 1414 resides effectively in parallel with the drain and source terminals of the NMOS transistor 1404.

The body of the NMOS transistor 1414 is typically tied to ground (or sometimes in lower frequency applications it is tied to the source terminal). In a triple well (or other) process the body of the NMOS transistor, which is the base of the parasitic NPN bipolar transistor, is available as a separate terminal. When the body is tied to ground, the parasitic NPN bipolar transistor is kept off. Under high electric field conditions, hole-electron pair generation in the high-field region close to the drain can inadvertently turn on the parasitic NPN bipolar transistor causing an undesired avalanche effect and snap back behavior in the device.

According to the present invention, the base of the parasitic NPN bipolar transistor 1414 is brought out so that it may be separately controlled to enhance the operation of an amplifier that employs the NMOS transistor 1404. In particular, a base contact 1412 of the parasitic NPN bipolar transistor 1414 is brought out using a P+ junction so that a bias voltage (VB) may be controllably applied thereto. By bringing out the body terminal (the base of the parasitic NPN bipolar transistor 1414), the composite device may be used as a follower. Depending on the application, the gate voltage (V_{bc}) and the base voltage (VB) can be independently controlled, resulting in the parasitic NPN bipolar transistor 1414 being fully off to fully on and/or the NMOS device 1404 being fully off to fully on, as will be described further with reference to FIG. 17.

One amplifier structure that may employ the structure of FIG. 14 is the cascode amplifier. Two particular embodiments of cascode amplifiers using the structure of FIG. 14 are described in more detail with reference to FIGs. 15-16. In these implementations, the NMOS transistor 1404 and the parasitic NPN bipolar transistor 1414 together serve as the cascode device. With the cascode device, the highest current efficiency is achieved by controlling the parasitic NPN bipolar transistor 1414 while forcing off the NMOS transistor 1404 since the impedance provided by the cascode device would be 1/gm of the bipolar device (with the NMOS transistor 1404 off) where gm=Ic/VT and VT=kT/q. The operating characteristics of the cascode amplifier may be altered by altering VB and V_{bc} differently, e.g., both NMOS transistor 1404 and parasitic NPN bipolar transistor 1414 on, or NMOS transistor 1404 on and parasitic NPN bipolar transistor 1414 off, etc.

Note that the device of FIG. 14 may be alternately implemented as a PMOS transistor and parasitic PNP transistor. In such case, the PMOS transistor is formed in an N-well. This differing structure may be used as a cascode device or as another device in a fashion similar to that described with reference to the device of FIG. 14.

(Arya, text for FIGs. 1-14 is imported from BP3315)

FIG. 15 is a schematic diagram illustrating a technique for tying a base of a parasitic NPN bipolar transistor to ground via an external resistance. With this technique, the body (p-well 1402) of the NMOS transistor 1404 is tied to ground via an external path that is represented by the inherent substrate and contact resistance for the body (Rsub), an external routing resistance employed to connect the body to ground (Rext), and an inductance of the external connection (Lpkg). The body (p-well 1402) is tied to ground via this connection in an attempt to keep the parasitic NPN bipolar transistor 1414 turned

off to avoid avalanche breakdown. Avalanche breakdown occurs when, under high electric field conditions, hole-electron pair generation in the high-field region close to the drain 1410 injects holes into to the body of the device. The current created by such hole injection passes through Rsub and Rext and turns the parasitic NPN bipolar transistor 1414 on by forward biasing its Base-Emitter junction. This phenomena may lead to a positive feedback loop in which the collector of the parasitic bipolar transistor 1414 itself injects holes into the base Rsub and Rext resulting in the start of the avalanche breakdown phenomena. If the high electric field on the drain 1410 of the transistor is due to a high frequency ac signal (as opposed to just DC voltage) the inductor Lpkg can also play a role in turning the parasitic bipolar transistor 1414 on, particularly if the source terminal 1406 is not grounded.

FIG. 16 is a cross-section taken along the channel of an N-type Metal-Oxide-Silicon (NMOS) transistor illustrating a parasitic NPN bipolar transistor 1414 having a base contact 1412 directly coupled to a source 1406 of the NMOS transistor according to the present invention. With the structure of FIG. 16, the body terminal (p-well 1402) of the NMOS transistor 1404 is brought out via the base contact 1412 that is directly tied to the source 1406 of the NMOS transistor 1404. At low frequencies, such tying may reduce the gmb of the composite device (transconductance associated with the source body junction) and to reduce the body effect and the resultant increase in the threshold voltage of the NMOS transistor 1404. As will be described further with reference to FIGs. 17 and 18, this structure is employed with a power amplifier primarily in order to ensure that the parasitic bipolar NPN transistor 1414 is not inadvertently turned on. The connection between the base contact 1412 and the source 1406 is a direct connection

using a low metal layer, e.g., metal-1, metal-2, or a plug that resides upon a surface of the p-well 1402, base contact 1412, and source 1406. With this structure, Rext and Lpkg are eliminated and cannot contribute to the difference in potential between the base (p-well 1402) and emitter 1406 of the parasitic NPN bipolar transistor 1414. Rsub is made small by using proper multi-island laid out devices and many substrate contacts.

FIG. 17 is a schematic diagram illustrating a first embodiment of a singled ended cascode power amplifier 1700 having a MOS transistor and a parasitic NPN bipolar transistor formed therewith and terminated according to the present invention. The single-ended cascode power amplifier 1700 has a structure similar to that of the single-ended cascode amplifier of FIG. 3 except that the cascode device has both a MOS transistor and a parasitic bipolar junction transistor formed in parallel therewith with a base of the parasitic bipolar transistor tied to a source of the MOS transistor. This structure may also include a peak detector and LPF 1108 and bias determination module 1110 that controls V_{bc}.

FIG. 18 is a schematic diagram illustrating a second embodiment of a singled ended cascode power amplifier 1800 having a parasitic NPN bipolar transistor terminated according to the present invention. The single-ended cascode power amplifier 1800 has a structure similar to that of the single-ended cascode amplifier of FIG. 4 except that the cascode device has both a MOS transistor and a parasitic bipolar junction transistor formed in parallel therewith and having with a base of the parasitic bipolar transistor tied to a source of the MOS transistor. The reader will appreciate that the structures of FIGs. 17 and 18 may serve as sides of differential cascode amplifiers, same or similar to the structures of FIGs. 5, 6, and 7. The structure of FIG. 18 may be employed in an amplifier

having an adjustable bias voltage Vbias applied to the gate of the NMOS transistor such as the structure illustrated in FIG. 6 or in FIG. 7.

As one of average skill in the art will appreciate, the term "substantially" or "approximately," as may be used herein, provides an industry-accepted tolerance to its corresponding term. Such an industry-accepted tolerance ranges from less than one percent to twenty percent and corresponds to, but is not limited to, component values, integrated circuit process variations, temperature variations, rise and fall times, and/or thermal noise. As one of average skill in the art will further appreciate, the term "operably coupled", as may be used herein, includes direct coupling and indirect coupling via another component, element, circuit, or module where, for indirect coupling, the intervening component, element, circuit, or module does not modify the information of a signal but may adjust its current level, voltage level, and/or power level. As one of average skill in the art will also appreciate, inferred coupling (i.e., where one element is coupled to another element by inference) includes direct and indirect coupling between two elements in the same manner as "operably coupled". As one of average skill in the art will further appreciate, the term "compares favorably", as may be used herein, indicates that a comparison between two or more elements, items, signals, etc., provides a desired relationship. For example, when the desired relationship is that signal 1 has a greater magnitude than signal 2, a favorable comparison may be achieved when the magnitude of signal 1 is greater than that of signal 2 or when the magnitude of signal 2 is less than that of signal 1.

The invention disclosed herein is susceptible to various modifications and alternative forms. Specific embodiments therefore have been shown by way of example

in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims.